What is claimed is:

1. An apparatus comprising:

an input circuit coupled to a first bus to transfer a delayed transaction (DT) data having a transaction identifier to one of N buffers, the input circuit being dynamically configured according to a bus frequency, N being a positive integer, the one of the N buffers being associated with the transaction identifier; and

an output circuit coupled to the buffers to transfer the DT data from the one of the N buffers to a second bus operating at the bus frequency, the output circuit being dynamically configured according to the bus frequency.

2. The apparatus of claim 1 wherein the input circuit comprises:

a 1-to-N de-multiplexing circuit to transfer the DT data from the first bus to the one of the N buffers based on the transaction identifier.

3. The apparatus of claim 2 wherein the output circuit comprises:

a N-to-1 multiplexing circuit to transfer the DT data from the one of the N buffers to the second bus based on the transaction identifier.

4. The apparatus of claim 3 wherein the 1-to-N de-multiplexing circuit comprises:

a 1-to-P de-multiplexer to transfer the DT data to one of P signal paths, P being a positive integers; and

P 1-to-Q de-multiplexers coupled to the P signal paths, Q being equal to N/P, each of the 1-to-Q de-multiplexers being coupled to Q of the N buffers to transfer the DT data to one of the Q buffers based on the transaction identifier.

5. The apparatus of claim 4 wherein each of the P 1-to-Q de-multiplexers transfers the DT data to the one of the Q buffers alternately.

6. The apparatus of claim 3 wherein the N-to-1 multiplexing circuit comprises:

P Q-to-1 multiplexers coupled to Q of the N buffers to transfer the DT data from one of the Q buffers to P signal paths based on the transaction identifier; and

a P-to-1 multiplexer coupled to the P Q-to-1 multiplexers via the P signal paths to transfer the DT data to the second bus.

7. The apparatus of claim 6 wherein each of the P Q-to-1 multiplexers transfers the DT data to the one of the Q buffers alternately.

8. The apparatus of claim 1 wherein the first bus is a primary bus coupled to a memory.

9. The apparatus of claim 1 wherein the second bus is one of a Peripheral Component Interconnect (PCI) bus and a PCI-X bus.

10. The apparatus of claim 9 wherein the delayed transaction data corresponds to a split transaction data when the second bus is the PCI-X bus.

11. A method comprising:

transferring a delayed transaction (DT) data having a transaction identifier to one of N buffers using an input circuit coupled to a first bus, the input circuit being dynamically configured according to a bus frequency, N being a positive integer, the one of the N buffers being associated with the transaction identifier; and

transferring the DT data from the one of the N buffers to a second bus operating at the bus frequency using an output circuit, the output circuit being dynamically configured according to the bus frequency.

12. The method of claim 11 wherein transferring the DT data to the one of N buffers comprises:

transferring the DT data from the first bus to the one of the N buffers based on the transaction identifier using a 1-to-N de-multiplexing circuit.

13. The method of claim 12 wherein transferring the DT data from the one of the N buffers comprises:

transferring the DT data from the one of the N buffers to the second bus based on the transaction identifier using a N-to-1 multiplexing circuit.

14. The method of claim 13 wherein transferring the DT data using the 1-to-N de-multiplexing circuit comprises:

transferring the DT data to one of P signal paths using a 1-to-P de-multiplexer, P being a positive integers; and

transferring the DT data to one of Q of the N buffers based on the transaction identifier using P 1-to-Q de-multiplexers coupled to the P signal paths, Q being equal to N/P, each of the 1-to-Q de-multiplexers being coupled to the Q buffers.

15. The method of claim 14 wherein transferring the DT data to one of the Q buffers comprises transferring the DT data to the one of the Q buffers alternately using each of the P 1-to-Q de-multiplexers.

16. The method of claim 13 wherein transferring the DT data from the one of the N buffers using the N-to-1 multiplexing circuit comprises:

transferring the DT data from one of the Q buffers to P signal paths based on the transaction identifier using P Q-to-1 multiplexers coupled to Q of the N buffers; and

transferring the DT data to the second bus using a P-to-1 multiplexer coupled to the P Q-to-1 multiplexers via the P signal paths.

17. The method of claim 16 wherein transferring the DT data to the second bus using a P-to-1 multiplexer comprises transferring the DT data to the one of the Q buffers alternately using each of the P Q-to-1 multiplexers.

18. The method of claim 11 wherein the first bus is a primary bus coupled to a memory.

19. The method of claim 11 wherein the second bus is one of a Peripheral Component Interconnect (PCI) bus and a PCI-X bus.

20. The method of claim 19 wherein the delayed transaction data corresponds to a split transaction data when the second bus is the PCI-X bus.

21. A system comprising:

a processor having a host bus;

a memory having a first bus;

a chipset coupled to the processor via the host bus and the memory via the first bus to control accesses to the memory from a device via a second bus operating at a bus frequency, the chipset having a buffer circuit, the buffer circuit comprising:

an input circuit coupled the a first bus to transfer a delayed transaction (DT) data having a transaction identifier to one of N buffers, the input circuit being dynamically configured according to the bus frequency, N being a positive integer, the one of the N buffers being associated with the transaction identifier, and

an output circuit coupled to the buffers to transfer the DT data from the one of the N buffers to the second bus, the output circuit being dynamically configured according to the bus frequency.

22. The system of claim 21 wherein the input circuit comprises:

a 1-to-N de-multiplexing circuit to transfer the DT data from the first bus to the one of the N buffers based on the transaction identifier.

23. The system of claim 22 wherein the output circuit comprises:

a N-to-1 multiplexing circuit to transfer the DT data from the one of the N buffers to the second bus based on the transaction identifier.

24. The system of claim 23 wherein the 1-to-N de-multiplexing circuit comprises:

a 1-to-P de-multiplexer to transfer the DT data to one of P signal paths, P being a positive integers; and

P 1-to-Q de-multiplexers coupled to the P signal paths, Q being equal to N/P, each of the 1-to-Q de-multiplexers being coupled to Q of the N buffers to transfer the DT data to one of the Q buffers based on the transaction identifier.

25. The system of claim 24 wherein each of the P 1-to-Q de-multiplexers transfers the DT data to the one of the Q buffers alternately.

26. The system of claim 23 wherein the N-to-1 multiplexing circuit comprises:

P Q-to-1 multiplexers coupled to Q of the N buffers to transfer the DT data from one of the Q buffers to P signal paths based on the transaction identifier; and

a P-to-1 multiplexer coupled to the P Q-to-1 multiplexers via the P signal paths to transfer the DT data to the second bus.

27. The system of claim 26 wherein each of the P Q-to-1 multiplexers transfers the DT data to the one of the Q buffers alternately.

28. The system of claim 21 wherein the second bus is one of a Peripheral Component Interconnect (PCI) bus and a PCI-X bus.

29. The system of claim 28 wherein the delayed transaction data corresponds to a split transaction data when the second bus is the PCI-X bus.